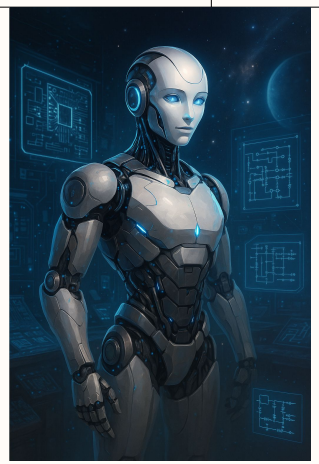
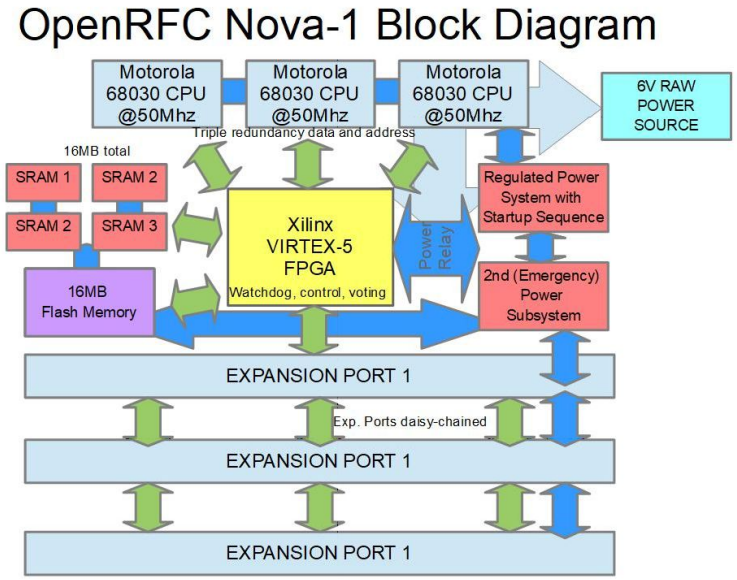


Nova Space Computer – System Overview

RFCOMPUTERS.NET

DESIGNED LIKE SPACE HARDWARE, WITH THE HELP OF MY A.I. COPILOT: NOVA
This board reflects real-world mission system practices:
- Modular, testable, and observable architecture
- Radiation-aware layout and signal protection
- Bus redundancy and graceful failure modes
- Flexible enough to be both a dev board and a working flight-like computer



Core Architecture
Triple Motorola MC68030 CPUs in lockstep mode:

Redundantly execute the same instructions.

Connected to the FPGA for voting and fault detection.

Each CPU has its own reset and halt control lines, with DIP-based fault injection (Chaos Switch 1).

FPGA Controller
Xilinx Virtex-5 XC5VLX50-1FFG676C:

Coordinates CPU lockstep and compares outputs.

Handles error monitoring, watchdog logic, and subsystem orchestration.

Controls Chaos Switches and emergency relays.

Powered through VCCINT (1.0 V), VCCAUX (1.8 V), and VCCO (3.3 V).

Memory System
Four CY7C1049GN30-10ZSXI 512k×8 asynchronous SRAMs:

Connected via address/data/control buses through SN74LVC245 bus buffers.

Buffers allow safe fault injection without compromising signal integrity.

Fixed direction from FPGA → RAM for injection; RAM → FPGA direct read.

⚡ Power Subsystem
Primary regulation via TPS65023RSBR Power Management Unit:

Generates 1.0 V, 1.8 V, and 3.3 V via internal DCDC converters.

Controlled power sequencing and monitoring.

Backup/emergency power:

Powered from an XT60 6 V input through MP1584EN-LF-Z buck regulators.

Controlled via relay circuit, activated by FPGA or Chaos Switch 3.

Diode-OR logic ensures safe fallback to emergency power.

Thermal Monitoring
6× LM75AD,118 digital temperature sensors:

I²C-connected to the FPGA.

Spread across key thermal zones for health monitoring.

☢ Radiation Pulse Detection

8× Vishay BPW34 PIN diodes + TLV7011DCKT comparators:

Fast analog pulse detection.

Output to FPGA for SEU/SEE detection.

Fault Injection & Resilience

Chaos Switch Bank 1: CPU faults (reset, halt, bus interference)

Chaos Switch Bank 2: RAM/address/data/FPGA faults

Chaos Switch Bank 3: Power subsystem manipulation (relay, DCDC enable override)

Manual DIP switches allow real-time fault injection for testing fault-tolerant architecture.

Programming & Configuration
Single JTAG port (M80-5000642) for FPGA configuration.

FPGA in Master BPI-Up boot mode from onboard 3.3 V NOR flash (e.g., S29GL128S90TFI020).

All configuration signals (M[2:0], INIT_B, DONE, etc.) properly terminated and monitored.

Expansion Ports – Overview

This system provides three high-density expansion ports, each using a 3-row 32-pin connector (650470-5). These are structured to give maximum flexibility and signal access to both internal buses and additional peripheral interfacing.

Port Layout & Capabilities
Each expansion port (J2, J3, J4) is composed of 3 blocks:

JxA (Rows A1–A32)

JxB (Rows B1–B32)

JxC (Rows C1–C32)

This gives 96 pins per expansion port, arranged in a way to support:

Full access to 32-bit data bus (CON_A/D0 – CON_A/D31)

Control signals such as CON_R/D, CON_W/R, CON_READY, CON_WAIT

SPI and I²C buses (CON_SPI_CLK, MOSI, MISO, CS, I2C_SCL, I2C_SDA)

Dedicated IO lines (CON_IO0 – CON_IO30)

Interrupt & handshake signals (CON_IRQx, CON_INT_ACK)

FPGA clock and latch lines (CON_FPGA_CLK, CON_A_LATCH)

JTAG programming lines for chained or external FPGA/JTAG access

Power rails: Each port has protected 3.3V (EMR_PWR_3V3) and 5V (EMR_PWR_5V0) via SS14 diodes for emergency power backup.

ESD & Protection
TVS Diodes (SMF5.0AT1G) are included on most signal lines for overvoltage protection.

All signal paths are matched and routed through resistor networks (typically 33 Ω) to provide basic impedance matching and fault tolerance.

Usage & Scenarios

These ports are designed for:

Connecting external co-processors or sensor modules

Testing and debugging via logic analyzers

Adding future expansion cards or custom peripherals

Interfacing with external memory banks or actuator controllers

Experimental connections to radiation-hardened daughterboards

Title	SUMMARY PAGE		
Size: A3	Number: 1		Revision: 0.1
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